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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,550	06/27/2003	Edward A. Burton	INTEL-021	7414
34610	7590	02/06/2006	EXAMINER	
FLESHNER & KIM, LLP				NGUYEN, DAO H
P.O. BOX 221200				ART UNIT
CHANTILLY, VA 20153				PAPER NUMBER
				2818

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/607,550	BURTON ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Dao H. Nguyen	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 10 November 2005.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 31-64 is/are pending in the application.
- 4a) Of the above claim(s) 35,38,40-47 and 57-64 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 31-34,36,37,39 and 48-56 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 March 2005 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

**DETAILED ACTION**

1. In response to the communications dated 05/23/2005 through 11/10/2005, claims 31-64 are active in this application.

Claims 1-30 have been cancelled.

Correction(s) to the drawing filed 03/14/2005 have been considered and accepted.

**Election/Restriction**

2. Application's election to prosecute the invention of Species II, claims 31-34, 36, 37, 39, and 48-56 for further prosecution.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election **without traverse** (MPEP § 818.03(a)).

Claims 35, 38, 40-47, and 57-64 is/are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

3. Applicant is reminded that a complete reply to the **final rejection** must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01. Also, upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

#### **Remarks**

4. Applicant's argument(s), filed 05/23/2005, have been fully considered, but are moot in view of the new ground(s) of rejection(s).

#### **Claim Rejections - 35 USC § 102**

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 31, 33, and 37 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by

U.S. Patent No. 6,664,634 to Thompson et al.

Regarding claim 31, Thompson discloses a semiconductor device, as shown in figs. 3, 6, and 17, comprising:

a first set of signal wires 220 distributed among at least first and second adjacent layers 280; and

a second set of signal wires 230 distributed among at least the first and second layers 280, the first and second sets 220/230 having a different number of signal wires (fig. 3A, fig. 6), with the signal wires in the first set being substantially parallel and arranged in a first pattern, and the signal wires in the second set being substantially parallel and arranged in a second pattern (col. 5, lines 36-42).

Regarding claim 33, Thompson discloses the semiconductor device wherein the first layer (lower layer) 280 has a number of signal wires from the first and second sets (which is/are equal to the total number of signal wires 220 of the first set) different from a number of signal wires from the first and second sets in the second layer (upper layer) 280 (which is/are equal to the total number of signal wires 230 of the second set). See figs. 3, 6, and 17.

Regarding claim 37, Thompson discloses the semiconductor device wherein the number of signal wires in the first (lower) layer 280 of the first set (which is/are equal to the total number of signal wires 220 of the first set) is different from the number of signal wires in the first layer of the second set (which is/are zero layer). See figs. 3, 6, and 17.

7. Claim(s) 31, 32, 34, 36, 39, and 49-56 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by admitted prior art (Admission).

Regarding claim 31, Admission discloses a semiconductor device, as shown in figs. 1-2 of the instant application, comprising:

a first set of signal wires 220 distributed among at least first and second adjacent layers 202/204, respectively; and

a second set of signal wires 230 distributed among at least the first and second layers 202/204, the first and second sets having a different number of signal wires, with the signal wires in the first set 220 being substantially parallel and arranged in a first pattern (left pattern between the left power supply 210 and the ground/return 212), and the signal wires in the second set 230 being substantially parallel and arranged in a second pattern (right pattern between the round/return 212 and the right power supply 210, fig. 2).

Regarding claim 32, Admission discloses the semiconductor device wherein each of the first and second sets 220/230 have an even number of signal lines. See fig. 2.

Regarding claim 34, Admission discloses the semiconductor device wherein the first and second patterns are a same pattern 200 (as a whole). See fig. 2.

Regarding claim 36, Admission discloses the semiconductor device wherein the first and second patterns are alternating patterns. See fig. 2.

Regarding claim 39, Admission discloses the semiconductor device wherein the first and second layers are adjoining layers. See figs. 1-2.

Regarding claim 49, Admission discloses the semiconductor device wherein the signal wires in the first set have a same permittivity and the signal wires in the second set have a same permittivity. This is inherent since they are formed of the same material.

Regarding claim 50, Admission discloses the semiconductor device wherein the first set of signal wires is separated from the second set of signal wires (by the ground/return 212). See fig. 2.

Regarding claim 51, Admission discloses the semiconductor device wherein the first set of signal wires 220 is separated from the second set of signal wires 230 by one or more ground or return wires 212. See fig. 2.

Regarding claims 52-56, Admission discloses the semiconductor device comprising all claimed limitations. See fig. 2.

8. Claim(s) 31-34, 36, 37, 39, and 48-50 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,466,892 to Howard et al.

Regarding claim 31, Howard discloses a semiconductor device, as shown in fig. 8, comprising:

a first set of signal wires 128/130/132/134 distributed among at least first and second adjacent layers 148/146; and

a second set of signal wires 140/142 (or 120/122) distributed among at least the first and second layers 148/146, the first and second sets having a different number of signal wires, with the signal wires in the first set being substantially parallel and arranged in a first pattern, and the signal wires in the second set being substantially parallel and arranged in a second pattern.

Regarding claim 32, Howard discloses the semiconductor device wherein each of the first and second sets have an even number of signal lines. See fig. 8.

Regarding claim 33, Howard discloses the semiconductor device wherein the first layer 148 has a number of signal wires from the first and second sets (which is/are equal to the total number of signal wires 128/130/132/134 of the first set) different from a number of signal wires from the first and second sets in the second layer 146 (which

is/are equal to the total number of signal wires 140/142 (or 120/122) of the second set).

See fig. 8.

Regarding claim 34, Howard discloses the semiconductor device wherein the first and second patterns are a same pattern 110. See fig. 8.

Regarding claim 36, Howard discloses the semiconductor device wherein the first and second patterns are alternating patterns. See fig. 8.

Regarding claim 37, Howard discloses the semiconductor device wherein the number of signal wires in the first layer 148 of the first set (which is/are equal to the total number of signal wires 128/130/132/134 of the first set) is different from the number of signal wires in the first layer of the second set (which is/are zero layer). See fig. 8.

Regarding claim 39, Howard discloses the semiconductor device wherein the first and second layers 148/146 are adjoining layers. See fig. 8.

Regarding claim 48, Howard discloses the semiconductor device wherein signal wires 128/130/132/134 in the first layer 148 are local interconnect wires and signal wires 120/122 in the second layer 146 are global routing wires. See fig. 8.

Regarding claim 49, Howard discloses the semiconductor device wherein the signal wires in the first set have a same permittivity and the signal wires in the second set have a same permittivity. This is inherent because they are identically formed.

Regarding claim 50, Howard discloses the semiconductor device wherein the first set of signal wires is separated from the second set of signal wires. See fig. 8.

### **Conclusion**

9. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If

attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen  
Art Unit 2818  
January 23, 2006



David Nelms  
Supervisory Patent Examiner  
Technology Center 2800